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Mano

Q.5.20: Design the sequential circuit specified by the state diagram of Fig. 5.19 using T flip-flops Q.

3.15: Simplify the following Boolean function F , together with the don't-care

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conditions d , and Q . 6.25:
It is necessary to generate six repeated timing signals T_0 through T_5 similar to the ones **Q. 5.1: The D latch of Fig. 5.6 is constructed with four NAND gates and an inverter. Consider the Q .**

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8.1: Explain in words and write HDL statements for the operations specified by the following ~~Morris Mano~~

~~Chapter 8 Problems~~ **Q. 2.15:**
Simplify the following Boolean functions T1 and T2 to a minimum number of

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literals. *Q. 7.15: Using $64 * 8$ ROM chips with an enable input, construct a $512 * 8$ ROM with eight chips and a*
Q. 3.16: Simplify the following functions, and implement them with two-level NAND gate circuits: Q.

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4.34: Implement the following Boolean function with a multiplexer (HDL—see Problem 4.48) Q. 5.8: Derive the state table and the state diagram of the sequential circuit shown in Fig. P5.8 state

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diagram/state table/circuit
diagram (using D-flip flop)
- Digital Logic Design

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*Combinational Logic
Circuits, Functions, \u0026
Truth Tables Q. 2.19:
Express following function
as sum of minterms and
product of maxterms: $F = B'D$
 $+ A'D + BD$ **Sequential
Circuit Analysis - From***

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**sequential circuit to state
transition diagrams.** *Latches
and Flip-Flops 1 - The SR
Latch*

Combinational circuit with
decoder and external logic
gates - Digital Electronics
Example

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Q. 4.27: A combinational circuit is specified by the following three Boolean functions

Q. 3.4: Simplify the following Boolean functions, using Karnaugh maps: (a) $F(x,y,z) = \text{sum}(2,3,6,7)$

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Q. 1.33: The state of a 12-bit register is 100010010111. What is its content if it represents Q.
5.4: A PN flip-flop has four operations: clear to 0, no change, complement, and set to 1, when

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Q. 3.9: Find all the prime
implicants for the following
Boolean functions, and

determine which are Q. 4.1:
*Consider the combinational
circuit shown in Fig.*

P4.1.(a) Derive the Boolean
expressions fo Computer*

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Logic Design M Morris Mano
Part 2 Q. 5.6: A sequential
circuit with two D flip-
flops A and B, two inputs, x
and y; and one output z is
Welcome to ... Solutions 3rd
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sequential circuit has three

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flip-flops A, B, C; one
input x_{in} ; and one output
 y_{out} .

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